Claims

What is claimed is:

1. A modulator capable of supporting two or more different modes of operation, each mode of operation corresponding to a different type of modulation, the modulator comprising:

an *m*-level phase shift keying (*m*-PSK) modulator including an input for receiving a serial data stream, and an output;

a phase rotator operatively coupled to the output of the *m*-PSK modulator for rotating a phase of an output signal generated by the *m*-PSK modulator by at least one of a first predetermined value corresponding to a first modulation type in a first mode of operation and a second predetermined value corresponding to a second modulation type in a second mode of operation;

a pulse shaping filter operatively coupled to the phase rotator; and

a controller operatively coupled to the phase rotator for selectively switching the modulator between the first and second modes of operation.

2. The modulator of claim 1, wherein *m* is equal to eight.

3. The modulator of claim 1, wherein the first modulation type is GMSK (Gaussian-filtered mean shift keying) and the second modulation type is EDGE (enhanced data rates for GSM evolution).

4. The modulator of claim 1, wherein the pulse shaping filter is configured to provide a linearized Gaussian response.

5. The modulator of claim 1, further comprising a transmit buffer operatively coupled to the input of the *m*-PSK modulator, the transmit buffer at least temporarily storing a portion of the serial data stream.

6. The modulator of claim 5, wherein the transmit buffer includes a serial-to-parallel converter for operatively transforming the serial data stream into triplets.

7. The modulator of claim 1, wherein the *m*-PSK modulator includes a read only memory (ROM) for storing a plurality of predetermined phases corresponding to the input data stream.

8. The modulator of claim 1, wherein the phase rotator comprises:

an adder including first and second inputs and an output, the first input of the adder being operatively coupled to the output of the *m*-PSK modulator; and

a ramp generator operatively coupled to the second input of the adder, wherein the ramp generator is responsive to the controller for selectively generating a phase ramp signal having at least one of a first slope in the first mode of operation and a second slope in the second mode of operation.

9. The modulator of claim 8, wherein the ramp generator comprises a counter for generating the phase ramp signal, the counter being programmable in response to the controller for operatively selecting a step size corresponding to at least one of the first slope and the second slope.

10. The modulator of claim 8, wherein the first slope is $\pi/2$ radians per step and the second slope is $3\pi/8$ radians per step.

11. The modulator of claim 1, wherein the pulse shaping filter includes a pulse amplitude modulator (PAM).

12. The modulator of claim 1, wherein the pulse shaping filter includes a finite impulse response (FIR) filter, the FIR filter including a predetermined number of taps wherein the taps are operatively configured to provide a linearized Gaussian response.

13. A semiconductor device for supporting two or more different types of modulation, the semiconductor device comprising:

a first modulator for performing a first type of modulation of an input data stream, the first modulator including one or more sub-circuits;

a second modulator for performing a second type of modulation of the input data stream, the second modulator including at least one sub-circuit that is common to the first modulator, the common sub-circuit operating in at least one of a first mode of operation corresponding to the first type of modulation and a second mode of operation corresponding to the second type of modulation; and

a controller operatively coupled to the first and second modulators, the controller being responsive to at least one control signal for selectively switching between one of at least the first and second modes of operation.

14. The semiconductor device of claim 13, wherein the first and second modulators include a common phase rotator, the phase rotator being responsive to the controller and operatively selecting one of at least a first phase rotation value in the first mode of operation and a second phase rotation value in the second mode of operation.

15. The semiconductor device of claim 14, wherein the first phase rotation value is $\pi/2$ radian and the second phase rotation value is $3\pi/8$ radian.

16. The semiconductor device of claim 13, wherein the first and second modulators include a common *m*-level phase shift keying (*m*-PSK) modulator, the *m*-PSK modulator being responsive to the controller and operatively selecting one of at least a first phase mapping in the first mode of operation and a second phase mapping in the second mode of operation.

17. The semiconductor device of claim 16, wherein *m* is equal to eight.

18. The semiconductor device of claim 13, wherein the first and second modulators include a common pulse shaping filter, the pulse shaping filter being configured to provide a linearized Gaussian response.

19. The semiconductor device of claim 13, wherein the first type of modulation is Gaussian mean shift keying (GMSK) and the second type of modulation is Enhanced Data Rates for GSM Evolution (EDGE).

20. A method for selectively modulating a signal in one of at least a first modulation type and a second modulation type, the method comprising the steps of:

providing an *m*-level phase shift keying (*m*-PSK) modulator, the *m*-PSK modulator operating in at least one of a first mode wherein the *m*-PSK modulator employs a first phase mapping corresponding to the first modulation type and a second mode wherein the *m*-PSK modulator employs a second phase mapping corresponding to the second modulation type;

modulating an input serial data stream using the *m*-PSK modulator in one of the first mode or the second mode of operation and generating an *m*-PSK-modulated signal;

rotating a phase of the *m*-PSK-modulated signal by one of a first predetermined phase rotation value in the first mode of operation and a second predetermined phase rotation value in the second mode of operation and generating a phase-rotated signal; and

filtering the phase-rotated signal using a pulse shaping filter.

21. The method of claim 20, wherein the pulse shaping filter is configured to provide a linearized Gaussian response.

22. The method of claim 20, further comprising the step of buffering the input serial data stream.

23. The method of claim 20, wherein the first type of modulation is Gaussian mean shift keying (GMSK) and the second type of modulation is Enhanced Data Rates for GSM Evolution (EDGE).